IN THE CLAIMS

Prior to examination of the above-referenced patent application, please amend the claims as follows.

1. (canceled).
2. (canceled).
3. (canceled).
4. (canceled).

5. (original) A power semiconductor device with trench gates comprising:
a semiconductor substrate;
a source layer at one surface of the substrate and comprising a high concentration of a dopant of one polarity;
a well layer beneath the source layer doped with a dopant of opposite polarity;
a plurality of trenches penetrating the source layer, said trenches substantially filled with conductive material;
a highly conductive layer on the surface of the source layer comprising a material reacted from a metal the semiconductor substrate;
an insulating layer on the highly conductive layer;
vias formed in the insulating layer and extending to the highly conductive layer on the source layer;
conductive material filling the vias for contacting the highly conductive layer.

6. (original) A method of forming an array of memory cells with each memory cell fabricated in and on a semiconductor body having a top surface, each memory cell comprising a vertical field effect transistor having a gate and first and second output regions separated by a channel region and a capacitor formed within a trench in the semiconductor body with a doped polysilicon first plate of the capacitor being partially surrounded by an insulating layer and being coupled to the second output region, which is formed by out-diffusion from the strap region and the first plate, through a doped polysilicon strap region with the insulating layer surrounding the first plate on all sides except for a selected portion of just one side of the first plate such that the second output region is limited in lateral extent to limit electrical leakage between second output regions of adjacent memory cells and the first output region

being self aligned to the channel region and the second output region, the second output region being formed by out-diffusion of impurities from the strap and first plate regions, starting at a point in which separated trenches have been formed in the semiconductor body and a relatively thin oxide layer has been formed at a bottom surface of each of the trenches and along lower portions of the sidewalls of the trenches which intersect the bottom surface of the trenches and a relatively thick layer of oxide has been formed on the remaining portions of the sidewalls, and the trenches are filled with a first doped polysilicon, the method comprising the step of using shallow trench isolation regions to define the lateral extent of each of the first output regions, and the lateral extent of each of the second output regions, the channel regions and the strap regions.

7. (original) A method of forming an array of memory cells with each memory cell fabricated in and on a semiconductor body having a top surface, each memory cell comprising a vertical field effect transistor having a gate and first and second output regions separated by a channel region and a capacitor formed within a trench in the semiconductor body with a doped polysilicon first plate of the capacitor being partially surrounded by an insulating layer and being coupled to the second output region, which is formed by out-diffusion from the strap region and the first plate, through a doped polysilicon strap region with the insulating layer surrounding the first plate on all sides except for a selected portion of just one side of the first plate such that the second output region is limited in lateral extent to limit electrical leakage between second output regions of adjacent memory cells and the first output region being self aligned to the channel region and the second output region, the second output region being formed by out-diffusion of impurities from the strap and first plate regions, starting at a point in which separated trenches have been formed in the semiconductor body and a relatively thin oxide layer has been formed at a bottom surface of each of the trenches and along lower portions of the sidewalls of the trenches which intersect the bottom surface of the trenches and a relatively thick layer of oxide has been formed on the remaining portions of the sidewalls, and the trenches are filled with a first doped polysilicon, the method comprising the steps of: etching the first doped polysilicon from an upper portion of each trench down to a level above the thin oxide covering the bottom portions of the sidewalls of the trenches; forming a layer of silicon nitride over the exposed portions of the relatively thick oxide layer

and a top surface of the remaining portion of the doped polysilicon; filling portions of the trenches lined with the layer of silicon nitride with a second doped polysilicon; forming shallow trench isolation regions extending from a top surface of the semiconductor body into the semiconductor body to partially define locations therein in which the first output region and the channel region of the transistor and the strap region are to be formed; removing portions of the second doped polysilicon not covered by the shallow trench isolation regions down to the silicon nitride layer formed on the top surface of the previously remaining portion of the first doped polysilicon which forms the first plate of the capacitor to define two sides of the trench, one of which is to contain the strap region and the channel region and a portion of one side of the second output region; forming a mask to define which of the two sides of the trench previously defined will contain the strap region; removing portions of the silicon nitride layer not covered by the mask or by the remaining second doped polysilicon; removing an exposed portion of the relatively thick oxide layer which is on the sidewalls of the trenches down to and below a top surface of the remaining portion of the first doped polysilicon which forms the first plate of each of the capacitors; removing the mask; removing the silicon nitride layer from a sidewall of the trench and a top portion over the remaining portion of the first doped polysilicon which is to become the first capacitor plate so as to expose the thick oxide layer on a sidewall of the trench; and filling the region of the trench in which the strap region is to be formed with a third doped polysilicon to from the strap region.

8. (original) The method of claim 7 further comprising the steps of: covering a top of the strap region and an exposed top surface of the remaining portion of the first doped polysilicon which forms the first plate of the capacitor with an oxide layer; forming an oxide layer on the exposed sidewall of the trench above the strap region to form a gate oxide; and filling the trench with a conductive material which serves as the gate of the transistor.

9. (original) The method of claim 7 further comprising the step of ion implanting dopant ions into the top surface of the semiconductor body to form first output regions in portions of the semiconductor body not covered by the shallow trench isolation regions, the energy of the ions being sufficient to penetrate the layer of silicon nitride on portions of the top surface of the semiconductor body, but insufficient to penetrate

the shallow trench isolation regions on other portions of the top surface of the semiconductor body, said first output regions being of a conductivity type opposite to that of the semiconductor body, and the channel and first and second output regions and the strap regions being all aligned to the shallow trench isolation regions.

10. (original) The method of claim 7 in which the material filling a trench in which a storage capacitor has been formed is patterned and used as an etch mask to define portions of the trench in which the channel region of a transistor and a strap region will be formed.

11. (canceled)

12. (canceled)

13. (canceled)

Respectfully submitted,

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